

## What is claimed is:

[Claim 1] 1. A method for automatic insertion and correctness verification of level shifters in a design of an integrated circuit (IC), wherein the IC comprises multiple voltage domains, the method comprising:

specifying a plurality of voltage constraints, defining at least one pair of voltage domains in the design and at least one level shifter cell;  
for each pair of voltage domains, checking whether a signal crossing the voltage domains is connected to a level shifter;  
verifying the correctness in the design of an existing level shifter;  
generating a level shifter module for the crossing signal, when the crossing signal is not correctly shifted; and  
inserting the generated level shifter module in the design.

[Claim 2] 2. The method of claim 1, wherein the voltage constraints for each voltage domain include at least a working voltage level of the voltage domain.

[Claim 3] 3. The method of claim 2, wherein the voltage constraints for each level shifter cell include: a source voltage domain, a destination voltage domain, an input terminal, an output terminal, an enable terminal, and a voltage domain to insert the level shifter cell.

[Claim 4] 4. The method of claim 3, wherein the level shifter cell is part of the generated level shifter module.

[Claim 5] 5. The method of claim 1, wherein the level shifter module is in at least one of: a register transfer level (RTL) description and a netlist description.

[Claim 6] 6. The method of claim 1, wherein the design is at least one of a register transfer level (RTL) description and a netlist description.

[Claim 7] 7. The method of claim 1, wherein the voltage constraints are specified via a graphical user interface (GUI).

[Claim 8] 8. The method of claim 1, wherein the verifying of the correctness of the level shifter module comprises:

checking whether the voltage level of the crossing signal is shifted to a working voltage level of a destination voltage domain;  
generating an error report when at least one level shifter cell in the level shifter module is not connected to a common enabling signal;  
generating an error report when the common enabling signal of the level shifter cell is not connected to an always-on voltage domain; and  
generating an error report when not more than one instance of the level shifter module is found in the design.

[Claim 9] 9. The method of claim 8, wherein the error report comprises an error type and a cause of the error.

[Claim 10] 10. The method of claim 8, wherein the error report is provided to the user.

[Claim 11] 11. The method of claim 1, wherein the generating of the level shifter module comprises producing a description language code implementing the level shifter module.

[Claim 12] 12. The method of claim 11, wherein the description language comprises at least one of: Verilog, VHDL, and a combination of Verilog and VHDL.

[Claim 13] 13. The method of claim 12, wherein the description language code comprises instructions assuring that the voltage level of the crossing signal is appropriately shifted.

[Claim 14] 14. The method of claim 11, wherein the inserting of the level shifter module comprises:

instantiating the description language code to form an instance of the level shifter module;  
inserting the instance of the level shifter module in a voltage domain specified in the voltage constraints; and  
renaming output names of the voltage domain.

[Claim 15] 15. The method of claim 14, wherein the insertion of the level shifter is performed using back referencing analysis and a synthesized netlist.

[Claim 16] 16. The method of claim 15, wherein the synthesized netlist is created using a synthesis engine.

[Claim 17] 17. The method of claim 1, wherein the inserting of the level shifter module is preceded by verifying the correctness of the level shifter module placed in the design.

[Claim 18] 18. The method of claim 1, implemented at least in part by one of a computer aided design (CAD) system, a CAD program, a netlist voltage domain analysis tool, and a register transfer level (RTL) voltage domain analysis tool.

[Claim 19] 19. A computer program product for enabling a computer to implement operations for automatic insertion and correctness verification of level shifters in a design of an integrated circuit (IC), wherein the IC comprises multiple voltage domains, the computer program product comprising a computer readable medium and instructions on the computer readable medium, the operations comprising:

- specifying a plurality of voltage constraints, defining at least one pair of voltage domains in the design and at least one level shifter cell;
- for each pair of voltage domains, checking whether a signal crossing the voltage domains is connected to a level shifter;
- verifying the correctness in the design of an existing level shifter;
- generating a level shifter module for the crossing signal, when the crossing signal is not correctly shifted;
- inserting the generated level shifter module in the design.

[Claim 20] 20. The computer program product of claim 19, wherein the voltage constraints for each voltage domain include at least a working voltage level of the voltage domain.

[Claim 21] 21. The computer program product of claim 20, wherein the voltage constraints for each level shifter cell include: a source voltage domain, a destination voltage domain, an input terminal, an output terminal, an enable terminal, and a voltage domain to insert the level shifter cell.

[Claim 22] 22. The computer program product of claim 21, wherein the level shifter cell is part of the generated level shifter module.

[Claim 23] 23. The computer program product of claim 19, wherein the level shifter module is in at least one of: a register transfer level (RTL) description and a netlist description.

[Claim 24] 24. The computer program product of claim 19, wherein the design is at least one of a register transfer level (RTL) description and a netlist description.

[Claim 25] 25. The computer program product of claim 19, wherein the voltage constraints are specified via a graphical user interface (GUI).

[Claim 26] 26. The computer program product of claim 19, wherein the verifying of the correctness of the level shifter module comprises:

- checking whether the voltage level of the crossing signal is shifted to a working voltage level of a destination voltage domain;
- generating an error report when at least one level shifter cell in the level shifter module is not connected to a common enabling signal;
- generating an error report when the common enabling signal of the level shifter cell is not connected to an always-on voltage domain; and
- generating an error report when not more than one instance of the level shifter module is found in the design.

[Claim 27] 27. The computer program product of claim 26, wherein the error report comprises an error type and a cause of the error.

[Claim 28] 28. The computer program product of claim 26, wherein the error report is provided to the user.

[Claim 29] 29. The computer program product of claim 19, wherein the generating of the level shifter module comprises producing a description language code implementing the level shifter module.

[Claim 30] 30. The computer program product of claim 29, wherein the description language comprises at least one of: Verilog, VHDL, and a combination of Verilog and VHDL.

[Claim 31] 31. The computer program product of claim 30, wherein the description language code comprises instructions assuring that the voltage level of the crossing signal is appropriately shifted.

[Claim 32] 32. The computer program product of claim 29, wherein the inserting of the level shifter module comprises:

- instantiating the description language code to form an instance of the level shifter module;
- inserting the instance of the level shifter module in a voltage domain specified in the voltage constraints; and
- renaming output names of the voltage domain.

[Claim 33] 33. The computer program product of claim 32, wherein the insertion of the level shifter is performed using back referencing analysis and a synthesized netlist.

[Claim 34] 34. The computer program product of claim 33, wherein the synthesized netlist is created using a synthesis engine.

[Claim 35] 35. The computer program product of claim 19, wherein the inserting of the level shifter module is preceded by verifying the correctness of the level shifter module placed in the design.

[Claim 36] 36. The computer program product of claim 19, implemented at least in part by one of a computer aided design (CAD) system, a CAD program, a netlist voltage domain analysis tool, and a register transfer level (RTL) voltage domain analysis tool.

[Claim 37] 37. A computer system for automatic insertion and correctness verification of level shifter modules in a design of an integrated circuit (IC), the system comprising:

- a database of voltage constraints;
- a code generator generating description language code of the level shifter modules;
- an insertion unit instantiating and inserting each of the level shifter modules in a respective voltage domain; and
- a checking unit verifying the correctness of the level shifter modules.

**[Claim 38]** 38. The system of claim 37, wherein the insertion unit outputs one or more updated design files.

**[Claim 39]** 39. The system of claim 38, wherein the design files include at least one of a register transfer level (RTL) description and a synthesized netlist.

**[Claim 40]** 40. The system of claim 37, wherein the checking unit generates at least one of an error report and a success report.

**[Claim 41]** 41. The system of claim 37, further comprising a graphical user interface allowing a user to specify the voltage constraints.